

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1. (Cancelled)

1 2. (Currently Amended) ~~The A method according to Claim 1,~~
2 ~~wherein of operating a digital system having a processor and~~
3 ~~associated translation lookaside buffer (TLB), comprising the steps~~
4 ~~of:~~

5 ~~executing a plurality of program tasks within the processor;~~
6 ~~initiating a plurality of memory access requests in response~~
7 ~~to the plurality of program tasks;~~

8 ~~caching a plurality of translated memory addresses in the TLB~~
9 ~~responsive to the plurality of memory access requests;~~

10 ~~incorporating a task identification value with each translated~~
11 ~~memory address to indicate which of the plurality of program tasks~~
12 ~~requested the respective translated memory address;~~

13 ~~incorporating a shared indicator with each translated memory~~
14 ~~address to indicate when a translated memory address is shared by~~
15 ~~more than one of the plurality of program tasks;~~

16 ~~invalidating a portion of the plurality of translated memory~~
17 ~~address in the TLB in a manner that is qualified by the shared~~
18 ~~indicator in response to an invalidate TLB entry command issued~~
19 ~~from the processor;~~

20 said invalidate TLB entry command comprises an invalidate
21 shared TLB entry command; and

22 the step of invalidating in response to an invalidate shared
23 TLB entry command comprises invalidating a translated memory
24 address in the TLB only if the corresponding shared indicator
25 indicates the translated memory address is shared by more than one
26 of the plurality of program tasks.

1 3. (Currently Amended) ~~The A method according to Claim 1,~~
2 ~~wherein of operating a digital system having a processor and~~
3 ~~associated translation lookaside buffer (TLB), comprising the steps~~
4 ~~of:~~

5 executing a plurality of program tasks within the processor;
6 initiating a plurality of memory access requests in response
7 to the plurality of program tasks;

8 caching a plurality of translated memory addresses in the TLB
9 responsive to the plurality of memory access requests;

10 incorporating a task identification value with each translated
11 memory address to indicate which of the plurality of program tasks
12 requested the respective translated memory address;

13 incorporating a shared indicator with each translated memory
14 address to indicate when a translated memory address is shared by
15 more than one of the plurality of program tasks;

16 invalidating a portion of the plurality of translated memory
17 address in the TLB in a manner that is qualified by the shared
18 indicator in response to an invalidate TLB entry command issued
19 from the processor;

20 said invalidate TLB entry command comprises an invalidate task
21 TLB entry except shared command, said invalidate task TLB entry
22 except shared command identifying one of the plurality of program
23 tasks; and

24 the step of invalidating in response to an invalidate task TLB
25 except shared command comprises invalidating a translated memory
26 address in the TLB only if the corresponding task identification
27 value indicates the program task identified by said invalidate task
28 TLB entry except shared command and the corresponding shared
29 indicator indicates the translated memory address is not shared by
30 more than one of the plurality of program tasks.

Claims 4 to 16. (Canceled)

1 17. (Currently Amended) The A digital system of Claim 14,
2 wherein having a translation lookaside buffer (TLB), the TLB
3 comprising:

4 storage circuitry with a plurality of entry locations for
5 holding translated values, wherein each of the plurality of entry
6 locations includes a first field for a translated value and a
7 second field for an associated shared indicator;

8 a set of inputs for receiving a translation request;

9 a set of outputs for providing a translated value selected
10 from the plurality of entry locations;

11 control circuitry connected to the storage circuitry, wherein
12 the control circuitry is responsive to an invalidate TLB entry
13 command to invalidate entries within said storage circuitry
14 qualified by the shared indicator field;

15 said invalidate TLB entry command comprises an invalidate
16 shared TLB entry command; and

17 said control circuitry being responsive to an invalidate
18 shared TLB entry command comprises to invalidate a translated
19 memory address in the storage circuitry only if the corresponding
20 shared indicator indicates the translated memory address is shared
21 by more than one of the plurality of program tasks.

1 18. (Currently Amended) The A digital system of Claim 14,
2 wherein having a translation lookaside buffer (TLB), the TLB
3 comprising:

4 storage circuitry with a plurality of entry locations for
5 holding translated values, wherein each of the plurality of entry
6 locations includes a first field for a translated value and a
7 second field for an associated shared indicator;

8 a set of inputs for receiving a translation request;

9 a set of outputs for providing a translated value selected
10 from the plurality of entry locations;
11 control circuitry connected to the storage circuitry, wherein
12 the control circuitry is responsive to an invalidate TLB entry
13 command to invalidate entries within said storage circuitry
14 qualified by the shared indicator field;
15 said storage circuitry wherein each of the plurality of entry
16 locations includes a third field for a task identification value;
17 said invalidate TLB entry command comprises an invalidate task
18 TLB entry except shared command, said invalidate task TLB entry
19 except shared command identifying one of a plurality of task
20 identification values; and
21 control circuitry being responsive to an invalidate task TLB
22 except shared command to invalidate a translated memory address in
23 the storage circuitry only if the corresponding task identification
24 value corresponds to said task identification value of said
25 invalidate task TLB entry except shared command and the
26 corresponding shared indicator indicates the translated memory
27 address is not shared.